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(54) Gain control in a QPSK demodulator

(57) Apparatus for automatic gain control of a QPSK demodulator comprising a variable gain amplifier for controlling the gain of a QPSK-demodulated signal by a gain control signal estimated using the equation

$S_{out} = MAX(|I|,|Q|) + \frac{1}{2}MIN(|I|,|Q|)$.

FIG.3

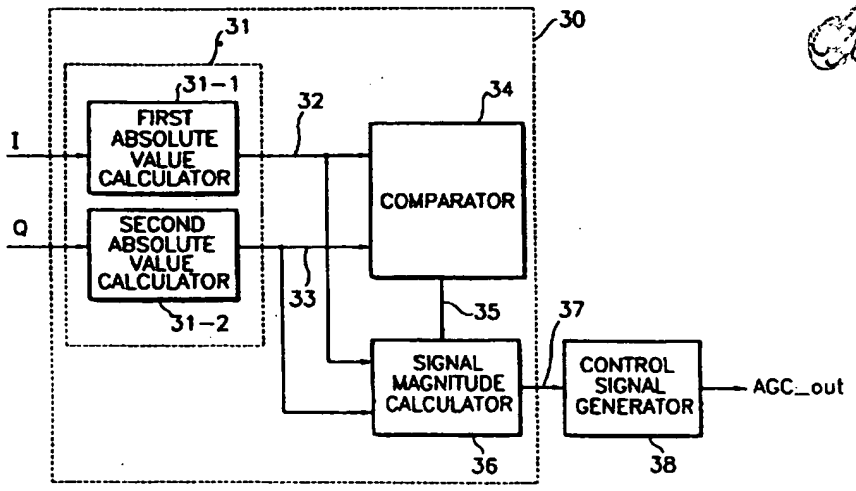

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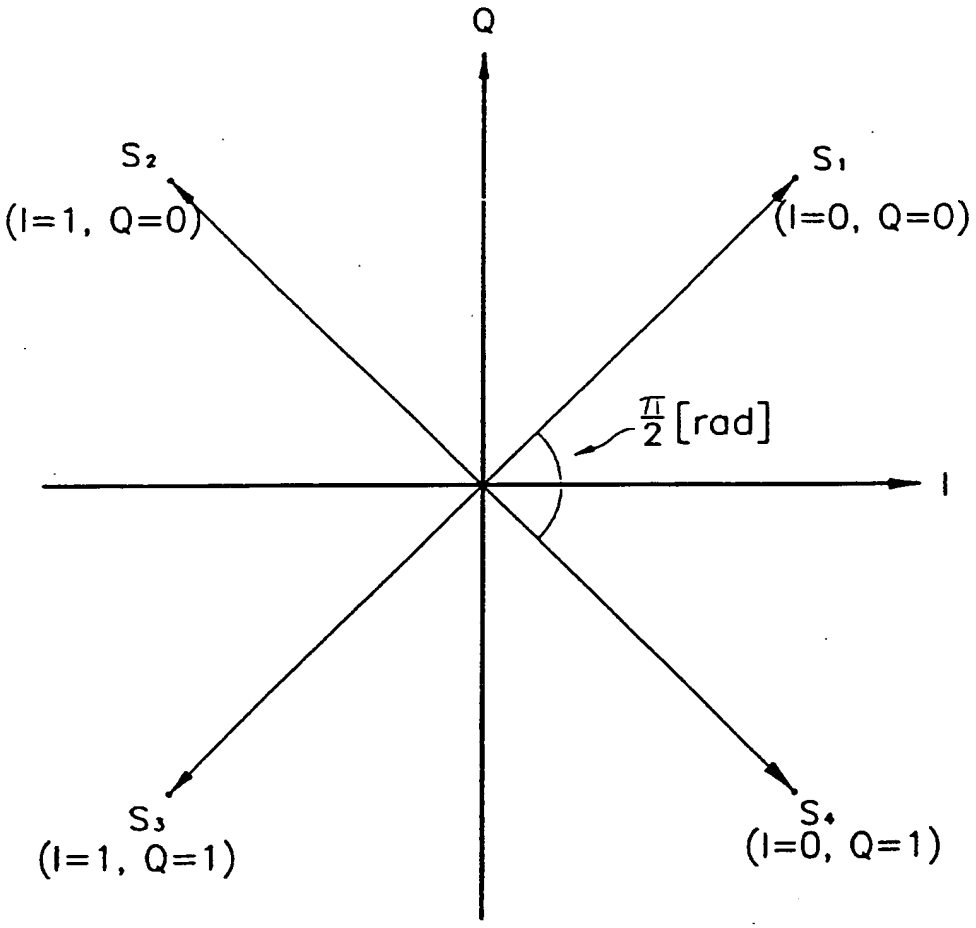
FIG. 1 (PRIOR ART)



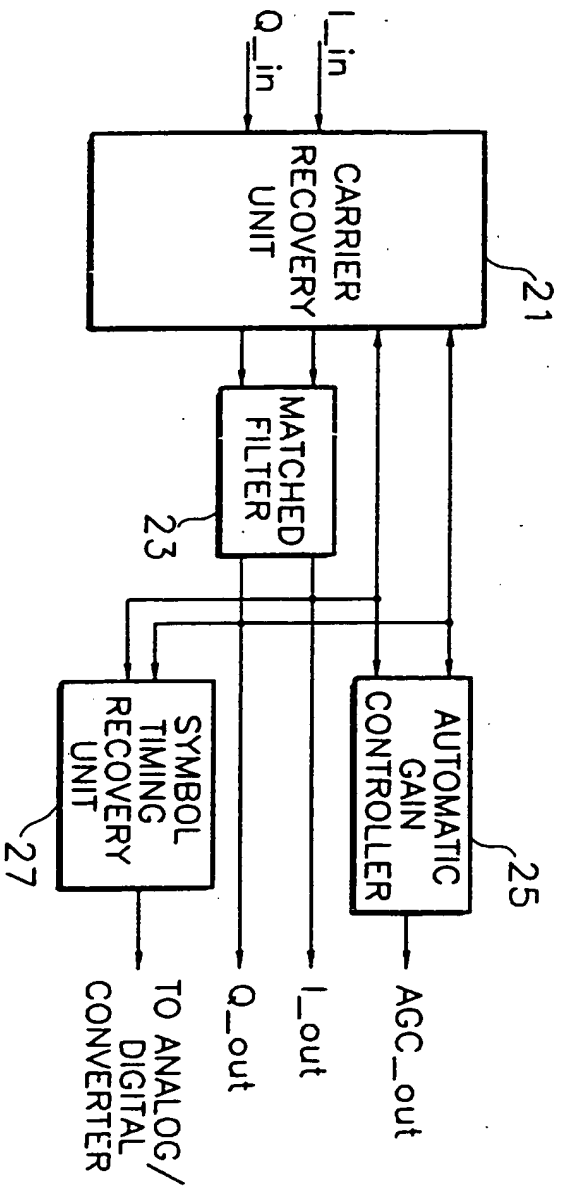


FIG.2(PRIOR ART)

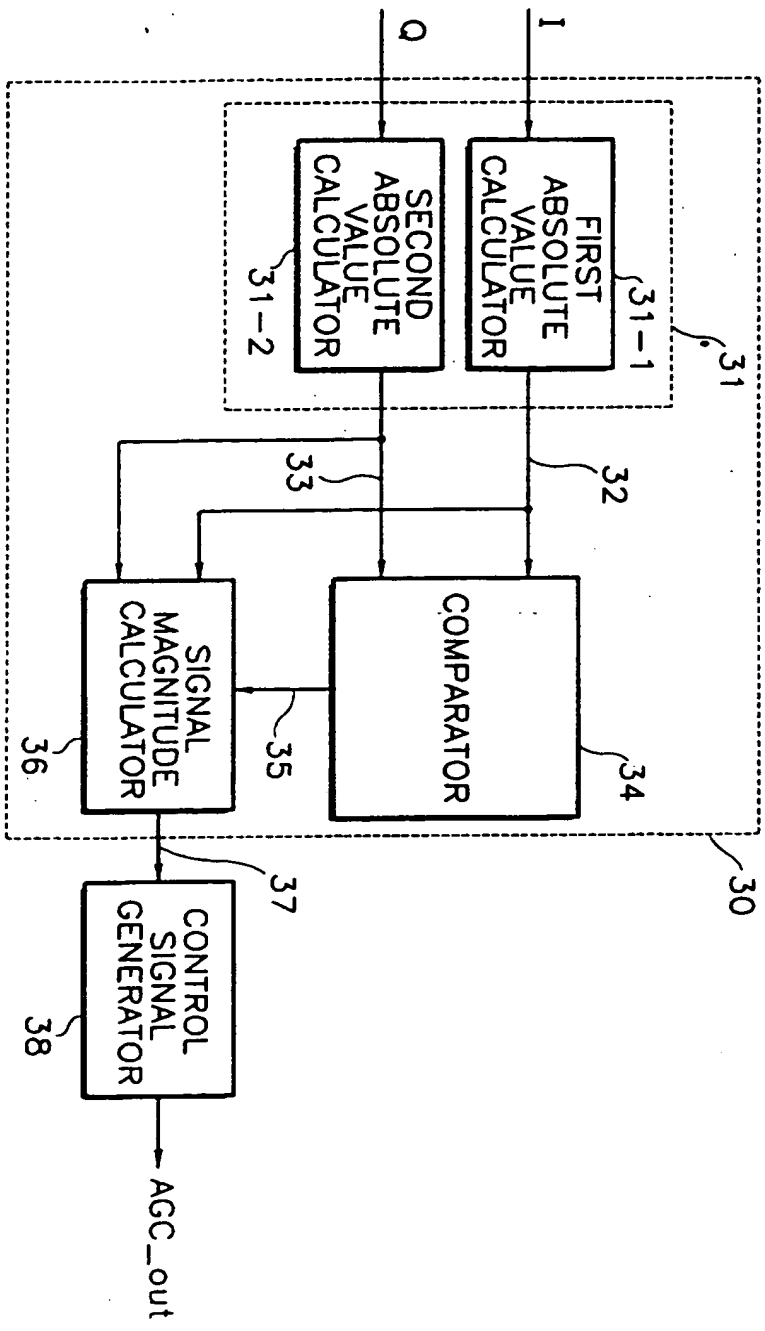

I
Q
FIRST ABSOLUTE VALUE CALCULATOR
SECOND ABSOLUTE VALUE CALCULATOR
31-1
31-2
31
32
33
COMPARATOR
SIGNAL MAGNITUDE CALCULATOR
34
35
36
37
CONTROL SIGNAL GENERATOR
38
30
AGC_out

FIG.3

FIG.4

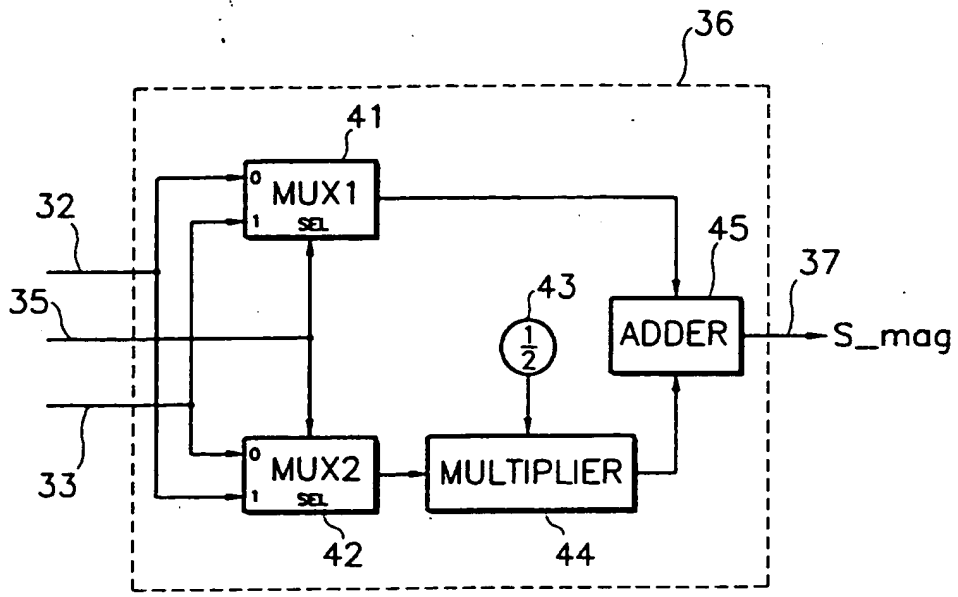
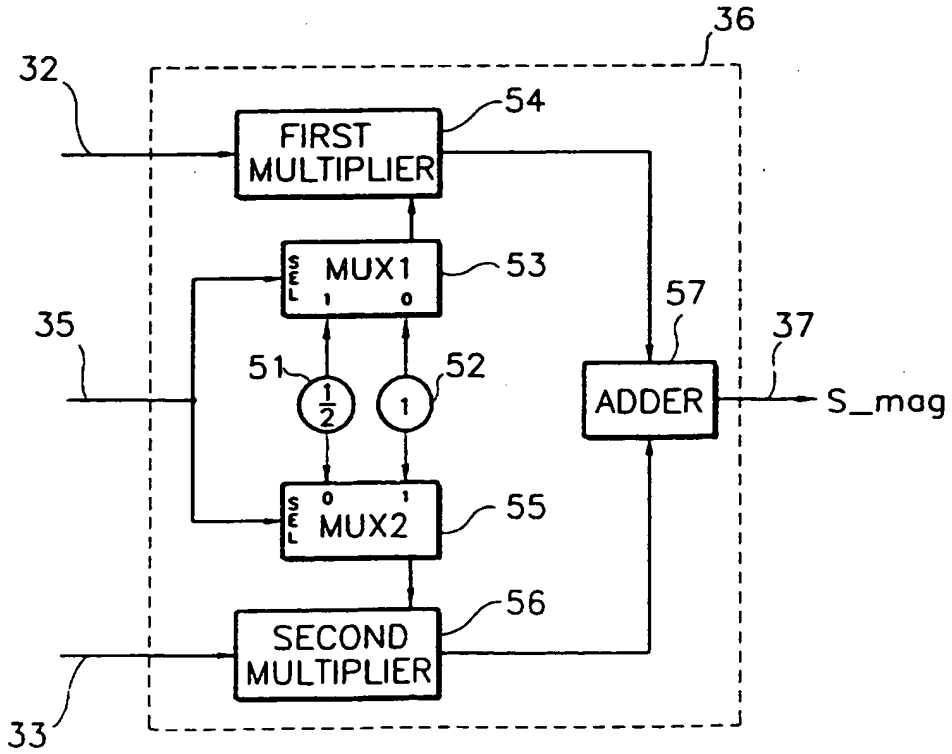

36
41
MUX1
SEL
32
35
33
45
37
43
ADDER
S_mag
MUX2
SEL
MULTIPLIER
42
44

FIG.5


36
32
FIRST MULTIPLIER
54
MUX1
SEL
53
35
57
37
51
52
ADDER
S_mag
MUX2
SEL
55
SECOND MULTIPLIER
56
33

METHOD AND APPARATUS FOR AUTOMATIC GAIN CONTROL IN QUADRATURE PHASE SHIFT KEYING DEMODULATOR

The present invention relates to a Quadrature Phase Shift Keying (QPSK) demodulator, and more particularly to a method and an apparatus for Automatic Gain Control (AGC) for obtaining the magnitude of signal inputted in the QPSK demodulator by square-root approximation, and adjusting an amplitude gain of QPSK demodulation signal according to the obtained magnitude of the input signal to maintain the magnitude of QPSK demodulated signal within the analog-to-digital convertible range.

In digital communication system, digital receivers for receiving a digitally modulated information signal conventionally comprise a variable gain amplifier with a gain adjusted by a control signal. The process for adjusting the gain of a received signal using a control signal is called the Automatic Gain Control (AGC). In general, the digital receiver requires measurement of an output signal power of the variable gain amplifier, which is carried out by the AGC process. The measured value is compared with a value representing a desired signal power. A gain control signal for the variable gain amplifier is generated according to the compared result. The gain control signal is then used to control an amplifier gain so that the output signal power of the variable gain amplifier coincide with the desired signal power. To perform digital demodulation with an optimum signal to noise (S/N) ratio. AGC is used to hold the magnitude of a baseband signal to the full dynamic range of an analog to digital (A/D) converter.

A Phase Shift Keying (PSK) demodulation used in the digital communication system is a method for shifting a phase of carrier to a predetermined value on a signal

space diagram according to the information signal. According to the number of phase in which the carrier has, the PSK demodulation is divided into a Binary Phase Shift Keying (BPSK) demodulation and a Quadrature Phase Shift Keying (QPSK) modulation. Between the two, QPSK is more widely used and Fig. 1 shows a QPSK bit mapping on a signal space diagram.

In Fig. 1, one symbol comprises an information signal, a 2-bits sequence and four symbols S_1, S_2, S_3, S_4 are positioned on each quadrant, and have a phase difference of $\pi/2$, respectively. When the signal is modulated, a bit signal corresponding to an in-phase channel (I-channel) is carried on a carrier $\cos\omega_0 t$ and a bit signal corresponding to an quadrature channel (Q-channel) is carried on a carrier $\sin\omega_0 t$, so that a superimposed signal between both signals is transmitted through the channel. In the receiver, the superimposed signal is inputted and the I-channel and Q-channel are divided by multiplying the inputted signal by $\cos\omega_0 t$ coincided with a frequency of the modulated carrier and a regenerated carrier of the $\sin\omega_0 t$, respectively. In comparison with the adjacent symbols having a different phase of $\pi/2$ radian, the QPSK modulated signal is mapped differently only by one-bit. and hence, a bit error rate generated by the phase is minimized when demodulating.

Fig. 2 shows a block diagram of a conventional QPSK demodulator. The QPSK demodulator comprises a carrier recovery unit **21**, a matched filter **23**, an automatic gain controller **25**. and a symbol timing recovery unit **27**.

In Fig. 2. in order to separate the I-channel signal **I_in** and the Q-channel signal **Q_in**. the carrier recovery unit **21** multiplies an I-channel signal **I_in** and a Q-channel signal **Q_in** of the baseband by $\cos\omega_0 t$ corresponding to the frequency of the modulated

carrier and the regenerated carrier of the $\sin\omega_0 t$, respectively. Further, the carrier recovery unit **21** detects a phase error value for each of the separated I and Q-channel, and also for pulse-shaped I and Q-channel signals fed-back from the matched filer **23**. It then outputs I and Q-channel signals with which the phase error is compensated to the matched filter **23**.

The matched filter **23** pulse-shapes the I and Q-channel signals outputted from the carrier recovery unit **21**, outputs final demodulated I and Q-channel signals **I_out** and **Q_out** to the carrier recovery unit **21**, the automatic gain controller **25**, and to the symbol timing recovery unit **27**.

The automatic gain controller **25** receives the final demodulated I and Q-channel signals **I_out** and **Q_out**, calculates the magnitude of signal inputted in the QPSK demodulator with respect to the I and Q-channel signal values, and generates a control signal **AGC_out** for adjusting a gain of an external or internal variable gain amplifier (not shown).

The symbol timing recovery unit **27** receives the final demodulated I and Q-channel signals **I_out** and **Q_out**, and generates an exact sampling clock from the detected timing error value for an analog/digital (A/D) converter (not shown).

Here, the calculated magnitude of input signal from the automatic gain controller **25** holds the level of the signal within input range of the A/D converter. Accordingly, the automatic gain controller **25** outputs the control signal **AGC_out** for increasing the gain if the magnitude of input signal from the QPSK demodulator is smaller than a predetermined reference value, whereas it outputs the control signal **AGC_out** for decreasing the gain if the magnitude of input signal from the QPSK demodulator is bigger than the predetermined reference value.

However, in the prior art, since the magnitude of signal for generating the control signal is calculated by a square-root formula, $\sqrt{(I^2 + Q^2)}$, a complex circuit is required to extract the square root, posing a difficult structural problem for an ASIC used in the QPSK demodulator.

In view of the foregoing, it is an object of the present invention to provide a method for automatic gain control, to calculate a magnitude of signal for generating a gain control signal to perform an AGC by using square-root approximation in a QPSK demodulator.

Another object of the present invention is to provide an apparatus for automatic gain control, to calculate the magnitude of signal for generating a gain control signal to perform an AGC by using square-root approximation in a QPSK demodulator for an efficient utilization of ASIC by eliminating the need of its complex circuitry.

In order to achieve the first object, the present invention provides the method for automatic gain control in a QPSK demodulator for demodulating a QPSK-modulated information signal according to a phase of a transmitted carrier, the method comprising:

a) calculating a magnitude of a signal inputted in the QPSK demodulator by using the equation $S_{mag} = MAX(|I|, |Q|) + \frac{1}{2} MIN(|I|, |Q|)$ from I and Q-channel signals inputted in the QPSK demodulator, where $|I|$ and $|Q|$ represent absolute values of I and Q-channel signals, respectively, S_{mag} represents the magnitude of the input signal, and *MAX(a,b)* and *MIN(a,b)* represent operators for selecting larger and smaller value between a and b, respectively; and

b) providing an external variable gain amplifier with a gain control signal generated according to the magnitude of the input signal obtained from the step a).

In order to achieve the another object, the present invention provides the apparatus for automatic gain control in a QPSK demodulator for demodulating a QPSK-modulated information signal according to a phase of a transmitted carrier, the apparatus comprising:

a signal magnitude estimator for estimating the magnitude of the I and Q-channel signals inputted in the QPSK demodulator by using the equation $S_{mag} = MAX(|I|,|Q|) + \frac{1}{2}MIN(|I|,|Q|)$; and

a control signal generator for generating a gain control signal according to the magnitude of the signal outputted from said signal magnitude estimator, and outputting the gain control signal to the variable gain amplifier.

The above and other objects, features, and advantages of the present invention will be apparent from the following detailed description of the preferred embodiments of the invention in conjunction with the accompanying drawings, in which:

Fig. 1 is a view illustrating four QPSK demodulation signals on a signal space diagram;

Fig. 2 is a block diagram illustrating a conventional QPSK demodulator;

Fig. 3 is a block diagram illustrating an apparatus for automatic gain control of the present invention in the QPSK demodulator;

Fig. 4 is a block diagram of a signal magnitude calculator illustrated in Fig. 3 in accordance with a first embodiment of the present invention; and

Fig. 5 is a block diagram of a signal magnitude calculator illustrated in Fig. 3 in accordance with a second embodiment of the present invention.

Reference will now be made in detail to the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

An apparatus for automatic gain control of the present invention illustrated in Fig. 3 is largely comprised by a signal magnitude estimator **30** for estimating a magnitude of signal inputted in a QPSK demodulator and a control signal generator **38**. The signal magnitude estimator **30** comprises an absolute value calculator **31** having a first absolute value calculator **31-1** and a second absolute calculator **31-2**, a comparator **34** for comparing both absolute values, and a signal magnitude calculator **36** for calculating the magnitude of signal from both absolute values according to a result of the comparison.

Referring to an operation of the apparatus for automatic gain control illustrated in Fig.3, the first and second absolute calculators **31-1** and **31-2** receive I and Q-channel signals and calculates their absolute values, respectively.

The comparator **34** receives absolute values **32** and **33** of I and Q-channel signals from the absolute value calculator **31**, compares both absolute values, and outputs a signal **35** according to a result of the comparison.

The signal magnitude calculator **36** receives absolute values **32** and **33** of I and Q-channel signals from the absolute value calculator **31**, adds a larger absolute value with 1/2 of a smaller absolute value according to a comparison result signal **35** from the comparator **34**, and outputs the sum as a magnitude of the signal.

Here, an approximation used to calculate the magnitude of signal S_{mag} in the present invention is derived from the following expressions 1 and 2.

Expression 1.

$$S_{mag} = \sqrt{(I^2 + Q^2)} = |I| \sqrt{(1 + (\frac{Q}{I})^2)}$$

$$\fallingdotseq |I|(1 + \frac{1}{2}\sqrt{(\frac{Q}{I})^2}) \fallingdotseq |I|(1 + \frac{1}{2}\frac{|Q|}{|I|})$$

$$= |I| + \frac{1}{2}|Q|$$

Expression 2.

$$S_{mag} = \sqrt{(I^2 + Q^2)} = |Q| \sqrt{(1 + (\frac{I}{Q})^2)}$$

$$\fallingdotseq |Q|(\frac{1}{2}\sqrt{(\frac{I}{Q})^2} + 1) \fallingdotseq |Q|(\frac{1}{2}\frac{|I|}{|Q|} + 1)$$

$$= |Q| + \frac{1}{2}|I|$$

In the above expressions 1 and 2, $|I|$ and $|Q|$ represent absolute values of I and Q- channel signals, respectively. The expression 1 is satisfied only if $|I|$ is larger than $|Q|$, and inversely, the expression 2 is satisfied only if $|Q|$ is larger than $|I|$.

Alternatively, the signal magnitude S_{mag} can be obtained by the following expression 3, which is a combined equivalent of the above two expressions.

Expression 3.

$$S_{mag} = MAX(|I|, |Q|) + \frac{1}{2}MIN(|I|, |Q|)$$

Here, ***MAX(a, b)*** and ***MIN(a, b)*** represent operators for selecting larger and smaller values between ***a*** and ***b***, respectively.

In brief, the magnitude of signal is obtained after comparing absolute values of I and Q-channel signals and adding the larger absolute value with 1/2 of the smaller absolute value.

The control signal generator **38** generates a gain control signal according to the magnitude of signal **37** obtained from the signal magnitude calculator **36**, and provides it to an internal or external variable gain amplifier (not shown).

Fig. 4 shows a block diagram of the signal magnitude calculator **36** illustrated in Fig. 3 in accordance with a first embodiment of the present invention. The signal magnitude calculator **36** comprises a first multiplexer **41**, a second multiplexer **42**, an adder **45**, a memory **43** for storing "1/2" value such as a ROM, a latch, or a mutiplier **44**.

The first multiplexer **41** selects and outputs a larger value of the absolute values **32** and **33** of I and Q-channel signals inputted in first and second input terminals **0** and **1**, respectively, according to the comparison result signal **35** from the comparator **34**. Namely, when the comparison result signal **35** represents the absolute value **32** of I-channel signal larger than the absolute value **33** of Q-channel signal, the first multiplexer **41** selects and outputs the absolute value **32** of I-channel signal. On the contrary, when the comparison result signal **35** represents the absolute value **32** of I-channel signal smaller than the absolute value **33** of Q-channel signal, the first multiplexer **41** selects and outputs the absolute value **33** of Q-channel signal.

The second multiplexer **42** selects and outputs a smaller value of the absolute values **33** and **32** of Q and I-channel signals inputted in first and second input terminals **0**

and 1, respectively, according to the comparison result signal 35 of the comparator 34. Namely, when the comparison result signal 35 represents the absolute value 32 of I-channel signal larger than the absolute value 33 of Q-channel signal, the second multiplexer 42 selects and outputs the absolute value 33 of Q-channel signal. On the contrary, when the comparison result signal 35 represents the absolute value 32 of I-channel signal smaller than the absolute value 33 of Q-channel signal, the first multiplexer 41 selects and outputs the absolute value 32 of I-channel signal.

Namely, the absolute value 32 of I-channel signal is applied to the first input terminal 0 of the first mutiplexer 41 and the second input terminal 1 of the second mutiplexer 42, and the absolute value 33 of Q-channel signal is applied to the second input terminal 1 of the first mutiplexer 41 and the first input terminal 0 of the second mutiplexer 42, so that the first and second multiplexers 41 and 42 selects and outputs the signal of the same input terminal according to the comparison result signal 35.

The multiplier 44 multiplies the smaller absolute value from the second multiplexer 42 by "1/2" value stored in the memory 43, and outputs the result.

The adder 45 adds the larger absolute value outputted from the first multiplexer 41 to the value obtained from the multiplier 44, and outputs this result as the magnitude of signal 37. Namely, the output from the adder 45 is $|I| + \frac{1}{2}|Q|$ when the absolute value 32 of I-channel signal is larger than the absolute value 33 of Q-channel signal, whereas $|Q| + \frac{1}{2}|I|$ when the absolute value 32 of I-channel signal is smaller than the absolute value 33 of Q-channel signal.

Fig. 5 shows a block diagram of the signal magnitude calculator **36** illustrated in Fig. 3 in accordance with a second embodiment of the present invention. The signal magnitude calculator **36** comprises a first memory **51** for storing "1/2" value such as a ROM or a latch, a second memory **52** for storing "1" value such as a ROM or a latch, a first multiplexer **53**, a first multiplier **54**, a second multiplexer **55**, a second multiplier **56**, and an adder **57**.

Now, an operation of the signal magnitude calculator **36** will be described in detail in connection with Fig. 3.

The first multiplexer **53** outputs selectively any one of "1" value from the second memory **52** inputted in the first input terminal **0** and "1/2" value from the first memory **51** inputted in the second input terminal **1**, according to a comparison result signal **35** from the comparator **34**, applied to a selection terminal **SEL**. Namely, when the comparison result signal **35** represents the absolute value **32** of I-channel signal larger than the absolute value **33** of Q-channel signal, the first multiplexer **53** outputs "1" value. On the contrary, when the comparison result signal **35** represents the absolute value **32** of I-channel signal smaller than the absolute value **33** of Q-channel signal, the first multiplexer **53** outputs "1/2" value.

The second multiplexer **55** outputs selectively any one of "1/2" value from the first memory **51** inputted in the first input terminal **0** and "1" value from the second memory **52** inputted in the second input terminal **1**, according to a comparison result signal **35** of the comparator **34** applied to the selection terminal **SEL**. Namely, when the comparison result signal **35** represents the absolute value **32** of I channel signal larger than the absolute value **33** of Q-channel signal, the second multiplexer **55** outputs "1/2" value. On the contrary, when the comparison result signal **35** represents the absolute value **32** of

I-channel signal smaller than the absolute value 33 of Q-channel signal, the second multiplexer 55 outputs "1" value.

Namely, the "1/2" value from the first memory 51 is input to the second input terminal 1 of the first multiplexer 53 and the first input terminal 0 of the second multiplexer 55, and the "1" value from the second memory 52 is input to the first input terminal 0 of the first multiplexer 53 and the second input terminal 1 of the second multiplexer 55. Accordingly, the first and second multiplexers 53 and 55 output selectively the signal of the same input terminal according to the comparison result signal 35.

The first multiplier 54 multiplies the absolute value 32 of I-channel signal by a constant value outputted from the first multiplexer 53, and outputs the result. Namely, the output from the first multiplier 54 is $|I|$ when the absolute value 32 of I-channel signal is larger than the absolute value 33 of Q-channel signal, whereas $\frac{1}{2}|I|$ when the absolute value 32 of I-channel signal is smaller than the absolute value 33 of Q-channel signal.

The second multiplier 56 multiplies the absolute value 33 of Q-channel signal by a constant value outputted from the second multiplexer 55, and outputs the result. Namely, the output from the second multiplier 56 is $\frac{1}{2}|Q|$ when the absolute value 32 of I-channel signal is larger than the absolute value 33 of Q-channel signal. whereas $|Q|$ when the absolute value 32 of I-channel signal is smaller than the absolute value 33 of Q-channel signal.

The adder 57 adds the output from the first multiplier 54 to the output from the

second multiplier **56**, and outputs the result as a magnitude of signal **37**. Namely, the output from the adder **57** is $|I| + \frac{1}{2}|Q|$ when the absolute value **32** of I-channel signal is larger than the absolute value **33** of Q-channel signal, whereas $|Q| + \frac{1}{2}|I|$ when the absolute value **32** of I-channel signal is smaller than the absolute value **33** of Q-channel signal.

As described above, in accordance with the apparatus and method for automatic gain control of the present invention, a hardware for using the square root approximation instead of a square root can be implemented when calculating the magnitude of input signal of QPSK demodulator for generating the gain control signal to perform AGC. Accordingly, the circuit structure of ASIC of the QPSK demodulator becomes simple for its effective utilization, and a time for calculating the magnitude of signal can be decreased.

While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiment, but, on the contrary, it is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims.

What is claimed is:

1. A method for automatic gain control in a QPSK demodulator for demodulating a QPSK-modulated information signal according to a phase of a transmitted carrier, characterized by comprising the steps of:

a) calculating a magnitude of I and Q-channel signals in the QPSK demodulator by using the equation $S_{mag} = MAX(|I|,|Q|) + \frac{1}{2}MIN(|I|,|Q|)$, where $|I|$ and $|Q|$ represent absolute values of I and Q-channels, respectively, S_{mag} represents the magnitude of the input signal, and ***MAX(a,b)*** and ***MIN(a,b)*** represent operators for selecting larger and smaller value between a and b, respectively; and

b) providing an external variable gain amplifier with a gain control signal generated according to the magnitude of the input signal obtained from the step a).

2. An apparatus for automatic gain control of a QPSK demodulator with a variable gain amplifier for controlling an amplification gain of a QPSK-demodulated signal by a predetermined gain control signal. characterized by comprising:

a signal magnitude estimator for estimating the magnitude of the I and Q-channel signals in the QPSK demodulator by using the equation $S_{mag} = MAX(|I|,|Q|) + \frac{1}{2}MIN(|I|,|Q|)$; and

a control signal generator for generating a gain control signal according to the magnitude of the signal outputted from said signal magnitude estimator. and outputting the gain control signal to the variable gain amplifier.

3. The apparatus for automatic gain control of claim 2, characterized in that said signal magnitude estimator comprises:

an absolute value calculator for calculating absolute values of the I and Q-channel signals, respectively;

a comparator for comparing both absolute values of the I and Q-channel signals; and

a signal magnitude calculator for calculating the magnitude of an input signal by adding a larger absolute value to 1/2 of a smaller absolute value according to a result of said comparator, said signal magnitude calculator comprising:

a first multiplexer for selecting and outputting a larger value of absolute values of I and Q-channel signals according to the result of said comparator;

a second multiplexer for selecting and outputting a smaller value of absolute values of I and Q-channel signals according to the result of said comparator;

a multiplier for multiplying the smaller absolute value inputted from said second multiplexer by "1/2" value and outputting the result; and

an adder for adding the larger value outputted from said first multiplexer to 1/2 of the smaller value outputted from said multiplier and outputting the result as a magnitude of the input signal.

4. The apparatus for automatic gain control of claim 3. characterized in that said signal magnitude calculator further comprises a memory for storing the "1/2" value.

5. The apparatus for automatic gain control of claim 2, characterized in that said signal magnitude estimator comprises:

an absolute value calculator for calculating absolute values of the I and Q-channel signals, respectively;

a comparator for receiving the absolute values of the I and Q-channel signals, respectively, and comparing the magnitude of both absolute values; and

a signal magnitude calculator for calculating the magnitude of an input signal by adding a larger absolute value to a smaller absolute value according to a comparison result of said comparator, said signal magnitude calculator comprising:

a first multiplexer for selectively outputting "1/2" or "1" value according to the comparison result of said comparator;

a first multiplier for receiving values outputted from said first multiplexer and an absolute value of the I-channel signal, and multiplying the both values;

a second multiplexer for outputting alternately "1/2" or "1" value to said first multiplexer according to the comparison result of said comparator;

a second multiplier for receiving a value outputted from said second multiplexer and an absolute value of the Q-channel signal, and multiplying the both values; and

an adder for receiving outputs from said first and second multipliers, adding both output values, and outputting the sum as a magnitude of the input signal.

6. The apparatus for automatic gain control of claim 5, characterized in that said signal magnitude calculator further comprises a first memory for storing the "1/2" value

and a second memory for storing the "1" value.

7. An apparatus for automatic gain control in a QPSK demodulator for demodulating a QPSK-modulated information signal according to a phase of a transmitted carrier, characterized by comprising:

a signal magnitude estimator for estimating the magnitude of the I and Q-channel signals in the QPSK demodulator by using the equation $S_{mag} = MAX(|I|,|Q|) + \frac{1}{2} MIN(|I|,|Q|)$; and

a control signal generator for generating a gain control signal according to the magnitude of the input signal outputted from said signal magnitude estimator, and outputting the gain control signal to an external variable gain amplifier.

8. A method for automatic gain control in a QPSK demodulator constructed and arranged substantially as herein described with reference to or as shown in the accompanying drawings.

9. An apparatus for automatic gain control in a QPSK demodulator constructed and arranged substantially as herein described with reference to or as shown in the accompanying drawings.

The Patent Office

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Application No: GB 9717538.4 **Examiner:** D. Midgley
Claims searched: 1-9 **Date of search:** 11 November 1997

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H3G GPXX,GSX

Int Cl (Ed.6): H03G 3/20,3/30 H04L 27/22,27/227,27/233

Other: ONLINE:WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	WO 95/30275 A1	(QUALCOMM) See, for example, page 15, paragraph 1	1,2,7
A	US 5083304	(MOTOROLA) See, for example, column 5, line 54 to column 6, line 4	"

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.